removing portions of said photoresist layer and portions of said plating seed layer of said at least one recess;

removing photoresist remaining in said at least one recess; and

electroplating a second metal to said plating seed layer in said recess without utilizing a mask.

16. (Amended) The method according to Claim 1, further comprising [the step of]:

removing said at least one conductive barrier layer from horizontal portions between aid recesses.

20.(Amended) The method of Claim 19, further comprising [the step of]:

forming a layer of at least one nitride or other passivation layer over the polyimide.

22.(Amended) A method for plating a second metal directly to a first metal, said method comprising [the steps of]:

providing a semiconductor substrate including at least one metal feature and at least one insulating layer covering said metal feature and said substrate;

forming at least one recess in said at least one insulating layer thereby exposing at least a portion of said metal feature;

forming at least one conductive barrier layer over said insulating layer and said exposed portion of said metal feature;

forming a plating seed layer of a first metal over said at least one barrier layer;

providing a pad in said at least one recess for preventing removal of portions of said seed layer in said at least one recess;

removing portions of said plating seed layer outside of said at least one recess;

removing said pad; and

electroplating a second metal to said plating seed layer in said recess without utilizing a mask.

23.(Amended) The method of claim 22, further comprising [the step of]:

utilizing a hard polishing pad to remove said seed layer outside of said recess.

Please add the following new claims:

24. A method for plating a second metal directly to a first metal, said method comprising:

providing a semiconductor substrate including at least one metal feature and at least one insulating layer covering said metal feature and said substrate;

forming at least one recess in said at least one insulating layer thereby exposing at least a portion of said metal feature;

forming at least one conductive barrier layer over said insulating layer and said exposed portion of said metal feature;

forming a plating seed layer of a first metal over said at least one barrier layer;

removing portions of said plating seed layer outside of said at least one recess; and

electroplating a second metal to said plating seed layer in said recess without utilizing a mask.

25. The method according to Claim 24, wherein said metal feature is a metal last provided in said semiconductor substrate.

26. The method according to Claim 24, wherein said conductive barrier is provided by sputter deposition of a layer of at least one nitride of tantalum on said insulating layer and said exposed portion of said metal feature and subsequent sputter deposition of a layer of tantalum on said tantalum nitride layer, such that the layer including the nitride of tantalum is in the α -phase.

27. The method according to Claim 26, wherein said tantalum nitride layer is about 10 Å to about 1000 Å thick and said tantalum layer is about 500 Å to about 5000 Å thick.

28. The method according to Claim 24, wherein said seed layer is formed by electrolytic or electroless plating of said first metal.

29. The method according to claim 28, wherein said seed layer is copper.

30. The method according to Claim 29, wherein said copper is sputter coated on said layer of tantalum.

31. The method according to Claim 30, wherein said layer of tantalum is α - Ta/TaN layer.

32. The method according to Claim 28, wherein said copper layer is about 1000 Å to about 20,000 Å thick.

33. The method according to claim 26, wherein said tantalum is alpha tantalum.

34. The method of Claim 26, wherein said tantalum layer is TaN/ α -Ta/TaN-laminate.

35. The method according to claim 24, wherein said seed layer outside of said recess is removed by chemical-mechanical polishing.

36. The method according to Claim 24, wherein said barrier layer forms a conductor for said electroplating of said second metal.

37. The method according to Claim 24, wherein said second metal is a solder ball made of an alloy of lead and tin, plated lead-free solder or other platable terminal metallurgies.

38. The method according to Claim 24, further comprising:

removing said at least one conductive barrier layer from horizontal portions between said recesses.

39. The method according to Claim 38, wherein said electroplated second metal acts as a mask for the removal of said at least one conductive barrier layer.

40. The method according to Claim 24, wherein said at least one metal feature is formed in said substrate.

41. The method according to Claim 24, wherein said insulating layer includes a layer of an oxide and a nitride and at least one layer of a polyimide.

42. The method of Claim 41 further comprising

forming a layer of at least one nitride or other passivation layer over the polyimide.

43. The method according to Claim 24, wherein said second metal is a solder ball.

44. The method according to Claim 22, wherein said metal feature is a metal last provided in said semiconductor substrate.

45. The method according to Claim 22, wherein said conductive barrier is provided by sputter deposition of a layer of at least one nitride of tantalum on said insulating layer and said exposed portion of said metal feature and subsequent sputter deposition of a layer of tantalum on said tantalum nitride layer, such that the layer including the nitride of tantalum is in the α-phase.

46. The method according to Claim 45, wherein said tantalum nitride layer is about 10 Å to about 1000 Å thick and said tantalum layer is about 500 Å to about 5000 Å thick.

47. The method according to Claim 22, wherein said seed layer is formed by electrolytic or electroless plating of said first metal.

48. The method according to Claim 47, wherein said seed layer is copper.

49. The method according to Claim 48, wherein said copper is sputter coated on said layer of tantalum.

50. The method according to Claim 49, wherein said layer of tantalum is α -Ta/TaN layer.

51. The method according to Claim 48, wherein said copper layer is about 1000 Å to about 20,000 Å thick.

52. The method according to Claim 45, wherein said tantalum is alpha tantalum.

53. The method of Claim 45, wherein said tantalum layer is TaN/ α -Ta/TaN-laminate.

54. The method according to Claim 22, wherein said portions of said seed layer outside of said recess are removed by chemical-mechanical polishing.

55. The method according to Claim 22, wherein said barrier layer forms a conductor for said electroplating of said second metal.

56. The method according to Claim 22, wherein said second metal is a solder ball made of an alloy of lead and tin, plated lead-free solder or other platable terminal metallurgies.